

A highly stable and low noise IMPATT oscillator at 75 GHz is realized by using the parametric injection locking technique along with an AFC circuit in which a crystal oscillator is used as a reference. Noise level of this oscillator is lower by 25 dB as compared with that of the free-running IMPATT oscillator and the frequency stability is as good as  $10^{-8}/^{\circ}\text{C}$ .

coefficient of the frequency  $\nu_0$  of the locked IMPATT oscillator is less than  $1.2 \cdot 10^{-8}/^\circ\text{C}$ , or the same order as that of the crystal oscillator used here.

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The block diagram of the circuit developed here is shown in Fig.1. Parts shown by thick lines are waveguide circuit (WRJ-740). A Si double-drift region (DDR) IMPATT diode is used in the oscillator, whose free-running frequency  $f_0$  is 75.5 GHz and the output power  $P_0$  is 16 dBm. An idler cavity is located at about  $8\lambda_g$  away from the diode, and its  $Q_{ext}$  is 2000. A signal from a varactor tuned transistor oscillator (1.5-1.7 GHz), which is designated as VFO, is injected through the bias circuit of the IMPATT oscillator. The IMPATT oscillator is then locked parametrically, and its sideband noise is reduced by more than 25 dB compared with that in the free-running state, as shown in Fig.2. The locking bandwidth is 700 MHz when the injection signal power is 23 dBm.

A part of the oscillation output is picked up and supplied to a frequency discriminating circuit, which produces a DC signal proportional to a drift  $\delta f'_0$  in the oscillation frequency  $f'_0$  of the locked IMPATT oscillator. This DC signal is fed back to the varactor in the VFO, thereby changing the injection signal frequency  $f_{inj}$  so as to cancel the drift  $\delta f'_0$  in the frequency  $f'_0$ . The loop gain of the AFC circuit is 30 or more.

The frequency discriminating circuit is constructed as follows. An output from a crystal oscillator (112.50 MHz) is multiplied by 16 times, and it locks a transistor oscillator (L.Osc.) at 1.80 GHz. The output of the latter is supplied to a step recovery diode (SRD), which produces many harmonic components. The 6th harmonic signal (10.80 GHz) is selected by a band pass filter, and supplied to a GaAs Schottky diode harmonic mixer. One of the mixing products between this reference signal (10.80 GHz) and the signal (75.53 GHz) from the locked IMPATT oscillator lies at or near 70 MHz, and it is amplified and supplied to a frequency discriminator, whose center frequency is set at 70 MHz and the bandwidth is 0.2 MHz.

When the ambient temperature  $T$  around the IMPATT oscillator and the idler cavity is changed by  $\delta T$ , the oscillation frequency  $f_0$  changed by  $\delta f$ , which can be measured by observing the signal ( $\sim 70$  MHz) from the harmonic mixer by using a spectrum analyzer. Fig.3 shows the measured data on  $\delta f$  v.s.  $\delta T$ . Although this curve is not a straight line,  $\delta f$  is only 10 KHz when  $\delta T$  is  $11^\circ\text{C}$ . This means that the temperature

Block diagram of the receiver system. The diagram shows a signal path starting from an IMPATT oscillator, passing through a circulator, a 75.53 GHz BPF, and a 10 dB coupler to the output. A feedback path branches off from the coupler, goes through a harmonic mixer (x7), a 10.80 GHz BPF, an SRD (x6), and an LOsc (x16) to a crystal oscillator (Xtal Osc) at 112.50 MHz. The feedback path also includes a DC Bias Source, a VFO at 1.6 GHz, an IF AMP (70 MHz), a Discriminator, and a DC AMP. A DC Bias of 0.3 mA is applied to the harmonic mixer. The output of the DC AMP is connected to a Spectrum Analyzer.

Fig.1 Block diagram of the circuit used here.

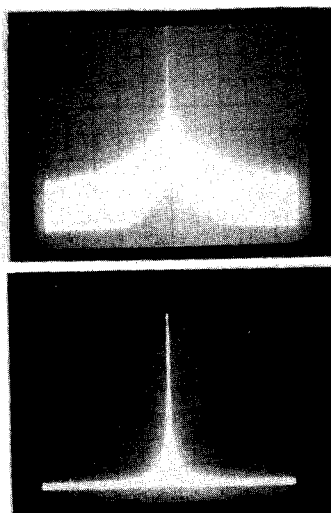


Fig. 2

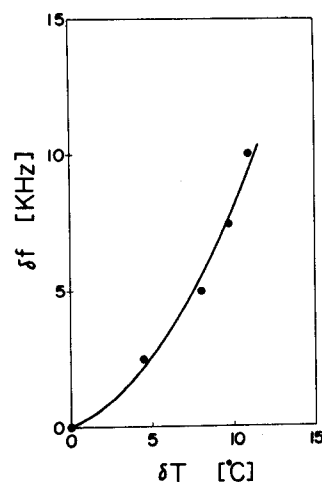


Fig. 3

Spectra of the oscillation output. Frequency shift v.s.  
Upper; free-running state. temperature change.  
Lower; locked state.  
Horizontal 1 MHz/div.  
Vertical 10 dB/div.